June 2006

National Semiconductor

LP3881
0.8A Fast-Response Ultra Low Dropout Linear Regulators

General Description

The LP3881 is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220, TO-263 and PSOP-8 packages.

Dropout Voltage: 75 mV (typ) @ 0.8A load current.

Ground Pin Current: 3 mA (typ) at full load.

Shutdown Current: 60 nA (typ) when S/D pin is low.

Precision Output Voltage: 1.5% room temperature accuracy.

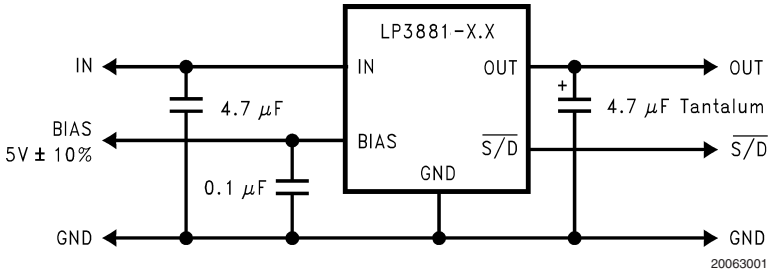
Features

- Ultra low dropout voltage (75 mV @ 0.8A typ)
- Low ground pin current
- Load regulation of 0.04%/A
- 60 nA typical quiescent current in shutdown
- 1.5% output accuracy (25˚C)
- TO-220, TO-263 and PSOP-8 packages
- Over temperature/over current protection
- –40˚C to +125˚C junction temperature range

Applications

- DSP Power Supplies
- Server Core and I/O Supplies
- PC Add-in-Cards
- Local Regulators in Set-Top Boxes
- Microcontroller Power Supplies
- High Efficiency Power Supplies
- SMPS Post-Regulators

Typical Application Circuit

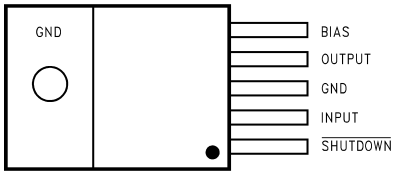


20063001

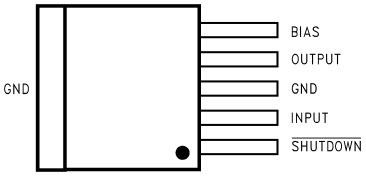
At least 4.7 µF of input and output capacitance is required for stability.

© 2006 National Semiconductor Corporation

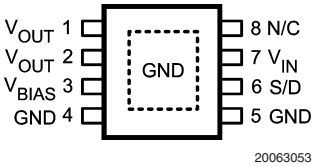
Connection Diagrams



TO-220, Top View



TO-263, Top View

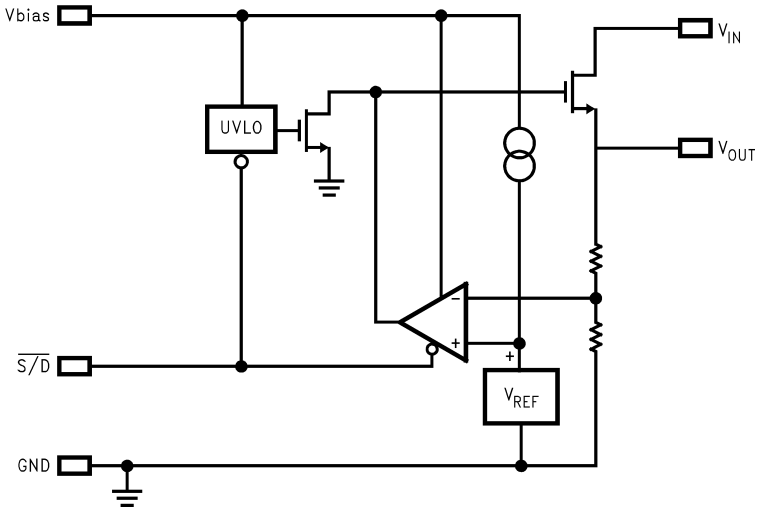


PSOP-8, Top View

Ordering Information

Order Number	Package Type	Package Drawing	Supplied As
LP3881ES-1.2	TO263-5	TS5B	Rail
LP3881ESX-1.2	TO263-5	TS5B	Tape and Reel
LP3881ET-1.2	TO220-5	T05D	Rail
LP3881ES-1.5	TO263-5	TS5B	Rail
LP3881ESX-1.5	TO263-5	TS5B	Tape and Reel
LP3881ET-1.5	TO220-5	T05D	Rail
LP3881ES-1.8	TO263-5	TS5B	Rail
LP3881ESX-1.8	TO263-5	TS5B	Tape and Reel
LP3881ET-1.8	TO220-5	T05D	Rail
LP3881EMR-1.2	PSOP-8	MRA08B	Rail
LP3881EMRX-1.2	PSOP-8	MRA08B	2500 Units on Tape and Reel
LP3881EMR-1.5	PSOP-8	MRA08B	Rail
LP3881EMRX-1.5	PSOP-8	MRA08B	2500 Units on Tape and Reel
LP3881EMR-1.8	PSOP-8	MRA08B	Rail
LP3881EMRX-1.8	PSOP-8	MRA08B	2500 Units on Tape and Reel

Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Lead Temp. (Soldering, 5 seconds)	260˚C
ESD Rating	
Human Body Model (Note 3)	2 kV
Machine Model (Note 10)	200V
Power Dissipation (Note 2)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +7V
Shutdown Input Voltage (Survival)	−0.3V to +7V
I_{OUT} (Survival)	Internally Limited
Output Voltage (Survival)	−0.3V to +6V
Junction Temperature	−40˚C to +150˚C

Operating Ratings

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to 5.5V
Shutdown Input Voltage	0 to +6V
I_{OUT}	0.8A
Operating Junction Temperature Range	−40˚C to +125˚C
V_{BIAS} Supply Voltage	4.5V to 6V

Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, $C_{IN} = C_{OUT}$ = 4.7 µF, $V_{S/D} = V_{BIAS}$.

Symbol	Parameter	Conditions	MIN (Note 5)	Typical (Note 4)	MAX (Note 5)	Units
V_O	Output Voltage Tolerance	10 mA < I_L < 0.8A $V_O(NOM) + 1V \le V_{IN} \le 5.5V$ $4.5V \le V_{BIAS} \le 6V$	1.198 **1.186**	1.216	1.234 **1.246**	V
			1.478 **1.455**	1.5	1.522 **1.545**	
			1.773 **1.746**	1.8	1.827 **1.854**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (Note 7)	$V_O(NOM) + 1V \le V_{IN} \le 5.5V$		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (Note 8)	10 mA < I_L < 0.8A		0.04 **0.06**		%/A
V_{DO}	Dropout Voltage (Note 9)	I_L = 0.8A (TO220 and TO263 only)		75	120 **160**	mV
		I_L = 0.8A (PSOP only)		80	140 **190**	
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 0.8A		3	7 **8**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 0.8A		1	2 **3**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V		2.5		A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON	**1.3**	0.7		V
		Output = OFF		0.7	**0.3**	
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)		20		µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)		15		
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V		1		µA
		$V_{\overline{S/D}} \le 0.3V$		−1		

Electrical Characteristics Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, $C_{IN} = C_{OUT}$ = 4.7 µF, $V_{S/D} = V_{BIAS}$. (Continued)

Symbol	Parameter	Conditions	MIN (Note 5)	Typical (Note 4)	MAX (Note 5)	Units
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT}$ +1V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz		70		
		$V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz		65		
	Output Noise Density	f = 120 Hz		1		µV/root–Hz
e_n	Output Noise Voltage V_{OUT} = 1.8V	BW = 10 Hz – 100 kHz		150		µV (rms)
		BW = 300 Hz – 300 kHz		90		

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. θ_{J-A} for TO-220 devices is 65˚C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a θ_{J-S} value of 4˚C/W can be assumed. θ_{J-A} for TO-263 devices is approximately 40˚C/W if soldered down to a copper plane which is at least 1.5 square inches in area. θ_{J-A} value for typical PSOP-8 PC board mounting is 166˚C/W. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.

Note 4: Typical numbers represent the most likely parametric norm for 25˚C operation.

Note 5: Limits are guaranteed through testing, statistical correlation, or design.

Note 6: If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

Note 7: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 8: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

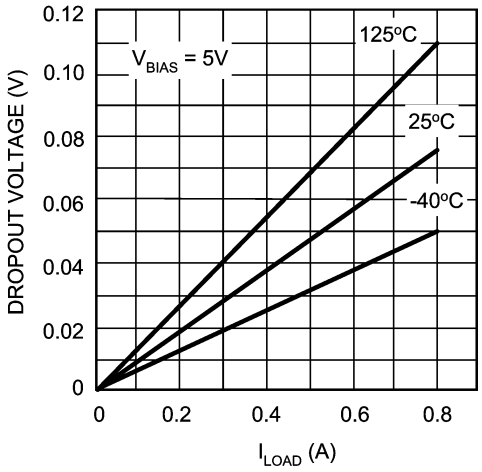
Note 9: Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value. The PSOP-8 package devices have a slightly higher dropout voltage due to increased band wire resistance.

Note 10: The machine model is a 220 pF capacitor discharged directly into each pin. The machine model ESD rating of pin 5 is 100V.

Typical Performance Characteristics

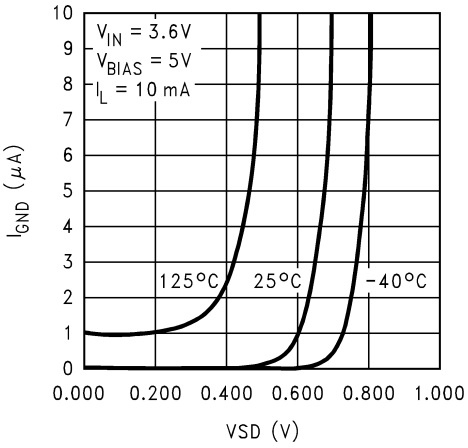
Unless otherwise specified: T_A = 25˚C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V

Dropout vs I_L



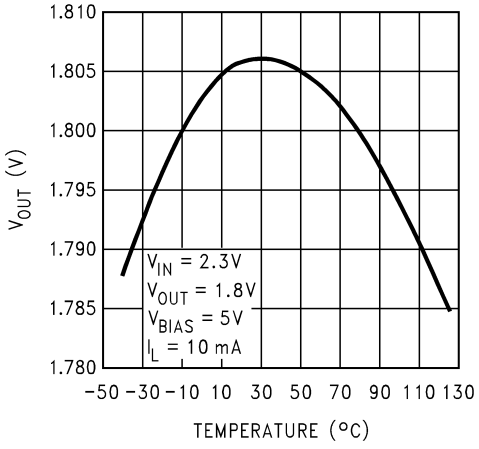
20063004

I_{GND} vs VSD



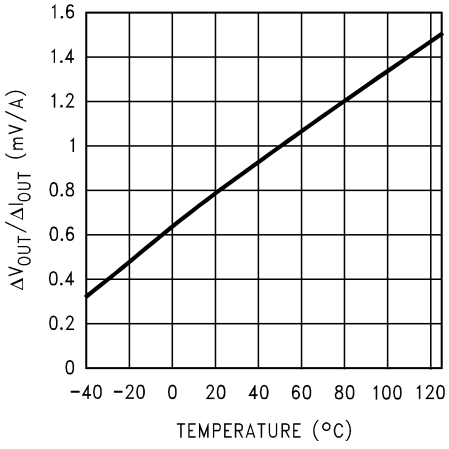
20063005

V_{OUT} vs Temperature



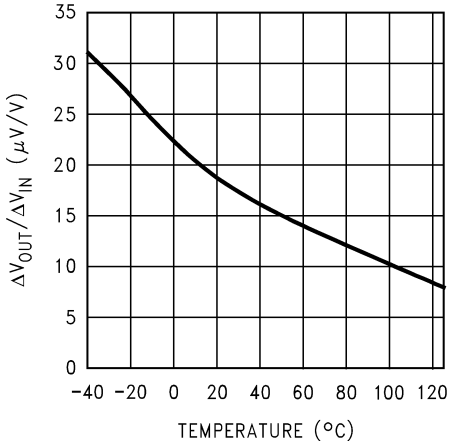
20063006

DC Load Regulation



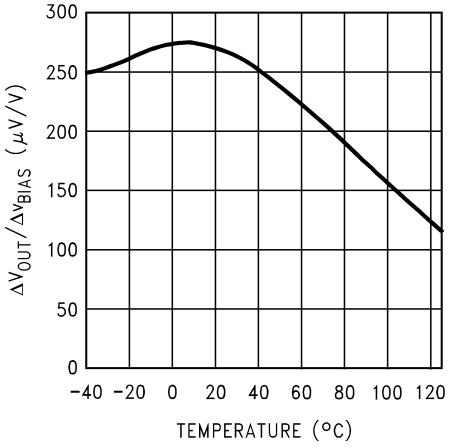
20063007

Line Regulation vs V_{IN}



20063008

Line Regulation vs V_{BIAS}

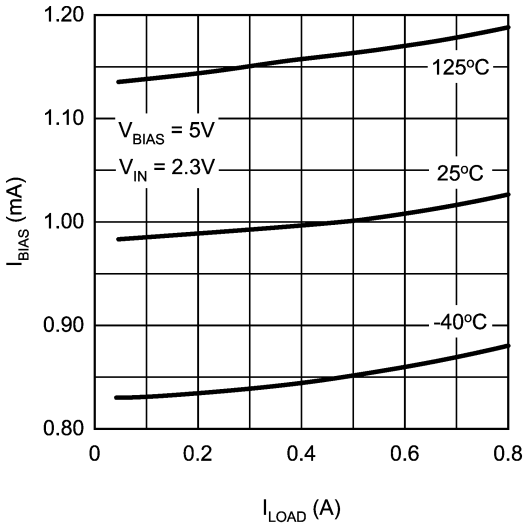


20063009

Typical Performance Characteristics

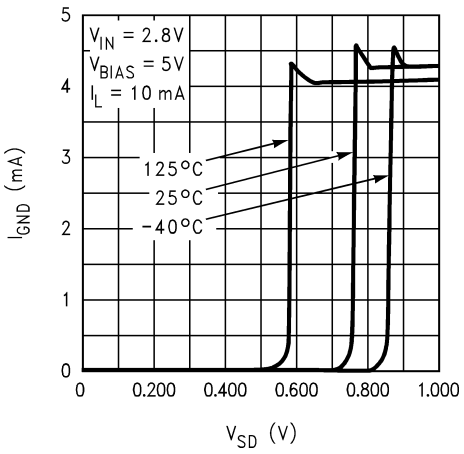
Unless otherwise specified: T_A = 25˚C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V (Continued)

I_{BIAS} vs I_L



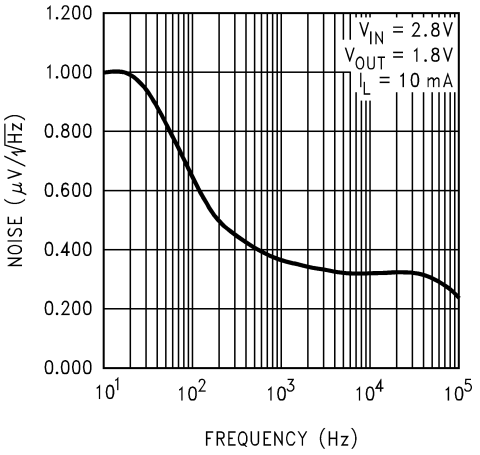
20063010

I_{GND} vs VSD



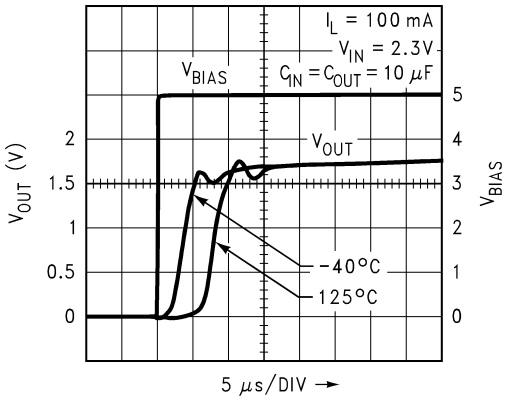
20063012

Noise Measurement



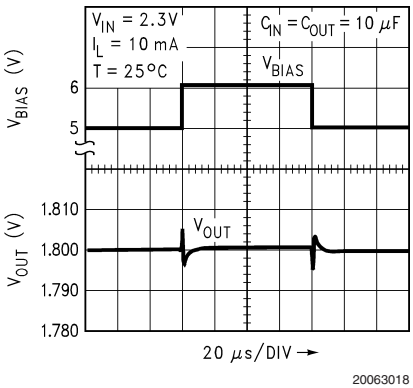
20063014

V_{OUT}Startup Waveform



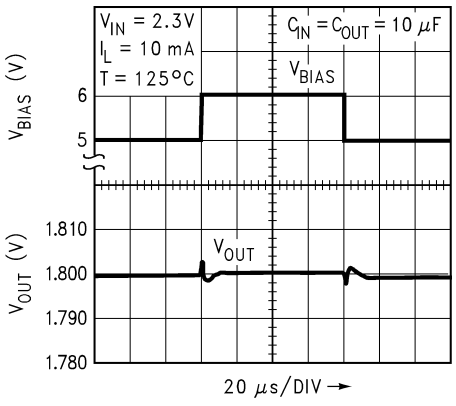
20063015

Line Regulation vs V_{BIAS}



20063018

Line Regulation vs V_{BIAS}

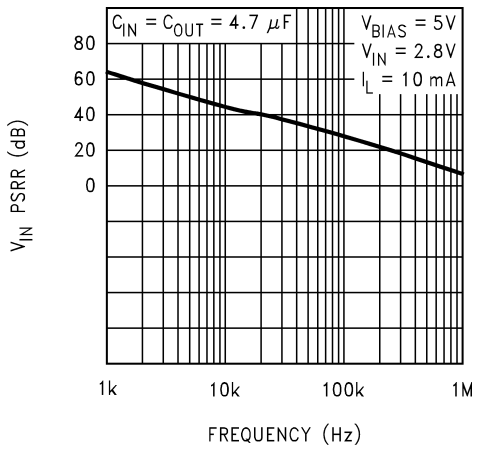


20063019

Typical Performance Characteristics

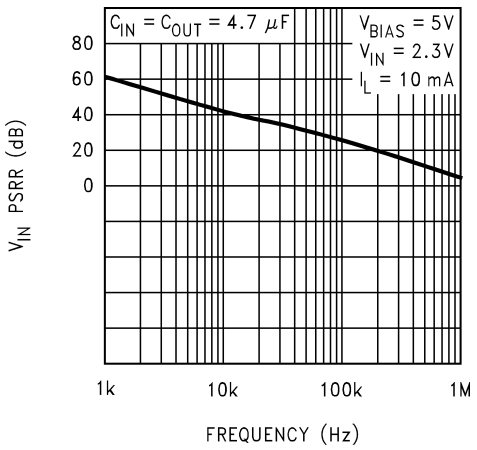
Unless otherwise specified: T_A = 25˚C, C_{OUT} = 4.7µF, Cin = 4.7µF, $\overline{S/D}$ pin is tied to V_{BIAS}, V_{IN} = 2.2V, V_{OUT} = 1.8V (Continued)

V_{IN} PSRR



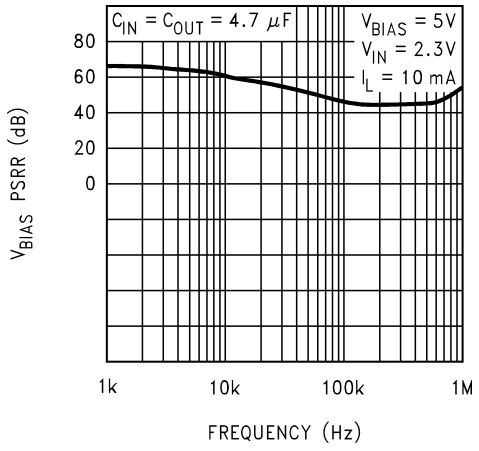
20063020

V_{IN} PSRR



20063023

V_{BIAS} PSRR



20063022

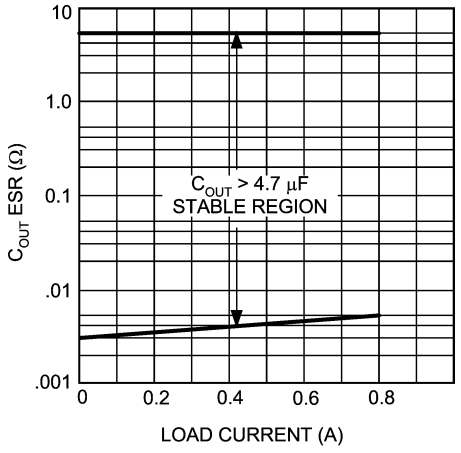
Application Hints

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

At least 4.7µF of output capacitance is required for stability (the amount of capacitance can be increased without limit). The output capacitor must be located less than 1 cm from the output pin of the IC and returned to a clean analog ground. The ESR (equivalent series resistance) of the output capacitor must be within the "stable" range as shown in the graph below over the full operating temperature range for stable operation.



Minimum ESR vs Output Load Current

Tantalum capacitors are recommended for the output as their ESR is ideally suited to the part's requirements and the ESR is very stable over temperature. Aluminum electrolytics are not recommended because their ESR increases very rapidly at temperatures below 10C. Aluminum caps can only be used in applications where lower temperature operation is not required.

A second problem with Al caps is that many have ESR's which are only specified at low frequencies. The typical loop bandwidth of a linear regulator is a few hundred kHz to several MHz. If an Al cap is used for the output cap, it must be one whose ESR is specified at a frequency of 100 kHz or more.

Because the ESR of ceramic capacitors is only a few milli Ohms, they are not suitable for use as output capacitors on LP388X devices. The regulator output can tolerate ceramic capacitance totaling up to 15% of the amount of Tantalum capacitance connected from the output to ground.

OUTPUT "BYPASS" CAPACITORS

Many designers place small value "bypass" capacitors at various circuit points to reduce noise. Ceramic capacitors in the value range of about 1000pF to 0.1µF placed directly on the output of a PNP or P-FET LDO regulator can cause a loss of phase margin which can result in oscillations, even when a Tantalum output capacitor is in parallel with it. This is not unique to National Semiconductor LDO regulators, it is true of any P-type LDO regulator.

The reason for this is that PNP or P-FET regulators have a higher output impedance (compared to an NPN regulator), which results in a pole-zero pair being formed by every different capacitor connected to the output.

The zero frequency is approximately:

$$F_z = 1 / (2 \times \pi \times ESR \times C)$$

Where ESR is the equivalent series resistance of the capacitor, and C is the value of capacitance.

The pole frequency is:

$$F_p = 1 / (2 \times \pi \times R_L \times C)$$

Where R_L is the load resistance connected to the regulator output.

To understand why a small capacitor can reduce phase margin: assume a typical LDO with a bandwidth of 1MHz, which is delivering 0.5A of current from a 2.5V output (which means R_L is 5 Ohms). We then place a .047 µF capacitor on the output. This creates a pole whose frequency is:

$$F_p = 1 / (2 \times \pi \times 5 \times .047 \times 10E\text{-}6) = 677 \text{ kHz}$$

This pole would add close to 60 degrees of phase lag at the crossover (unity gain) frequency of 1 MHz, which would almost certainly make this regulator oscillate. Depending on the load current, output voltage, and bandwidth, there are usually values of small capacitors which can seriously reduce phase margin. If the capacitors are ceramic, they tend to oscillate more easily because they have very little internal inductance to damp it out. If bypass capacitors are used, it is best to place them near the load and use trace inductance to "decouple" them from the regulator output.

INPUT CAPACITOR

The input capacitor must be at least 4.7 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. Ceramic capacitors work best for this, but Tantalums are also very good. There is no ESR limitation on the input capacitor (the lower, the better). Aluminum electrolytics can be used, but their ESR increase very quickly at cold temperatures. They are not recommended for any application where temperatures go below about 10˚C.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 6V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. Pin $\overline{S/D}$ must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

Application Hints (Continued)

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN}–V_{OUT})I_{OUT}+ (V_{IN})I_{GND}$

where I_{GND} is the operating ground current of the device.

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$T_{Rmax} = T_{Jmax}– T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JA} = T_{Rmax} / P_D$

These parts are available in TO-220 and TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 ˚C/W for TO-220 package and ≥ 60 ˚C/W for TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$\theta_{HA} \leq \theta_{JA} – \theta_{CH} – \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3˚C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5˚C/W to 2.5˚C/W. If the exact value is unknown, 2˚C/W can be assumed.

HEATSINKING TO-263 PACKAGE

The TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. The graph below shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

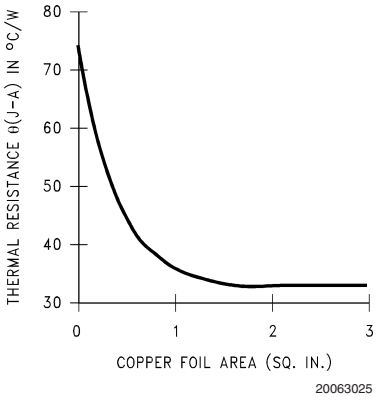


FIGURE 1. θ_{JA} vs Copper (1 Ounce) Area for TO-263 package

Application Hints (Continued)

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 package mounted to a PCB is 32˚C/W.

Figure 2 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35˚C/W and the maximum junction temperature is 125˚C.

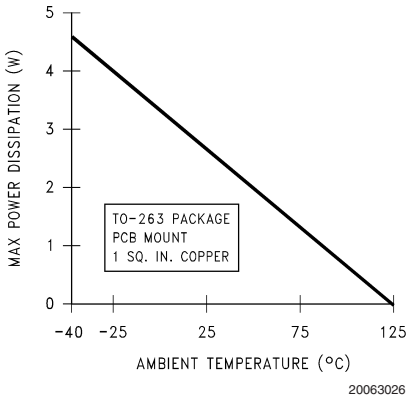


FIGURE 2. Maximum power dissipation vs ambient temperature for TO-263 package

HEATSINKING PSOP PACKAGE

Heatsinking for the PSOP-8 package is accomplished by allowing heat to flow through the ground slug on the bottom of the package into the copper on the PC board. The heat slug must be soldered down to a copper plane to get good heat transfer. It can also be connected through vias to internal copper planes. Since the heat slug is at ground potential, traces must not be routed under it which are not at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

Figure 3 shows a curve for the θ_{JA} of the PSOP package for different copper area sizes using a typical PCB with one ounce copper in still air.

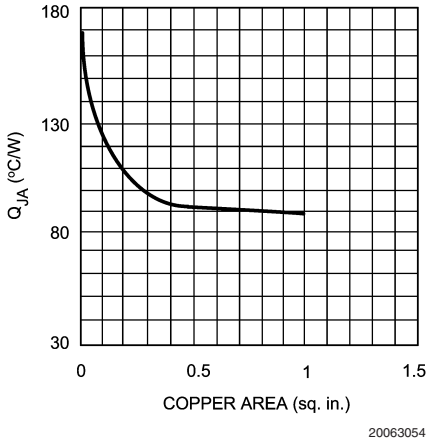
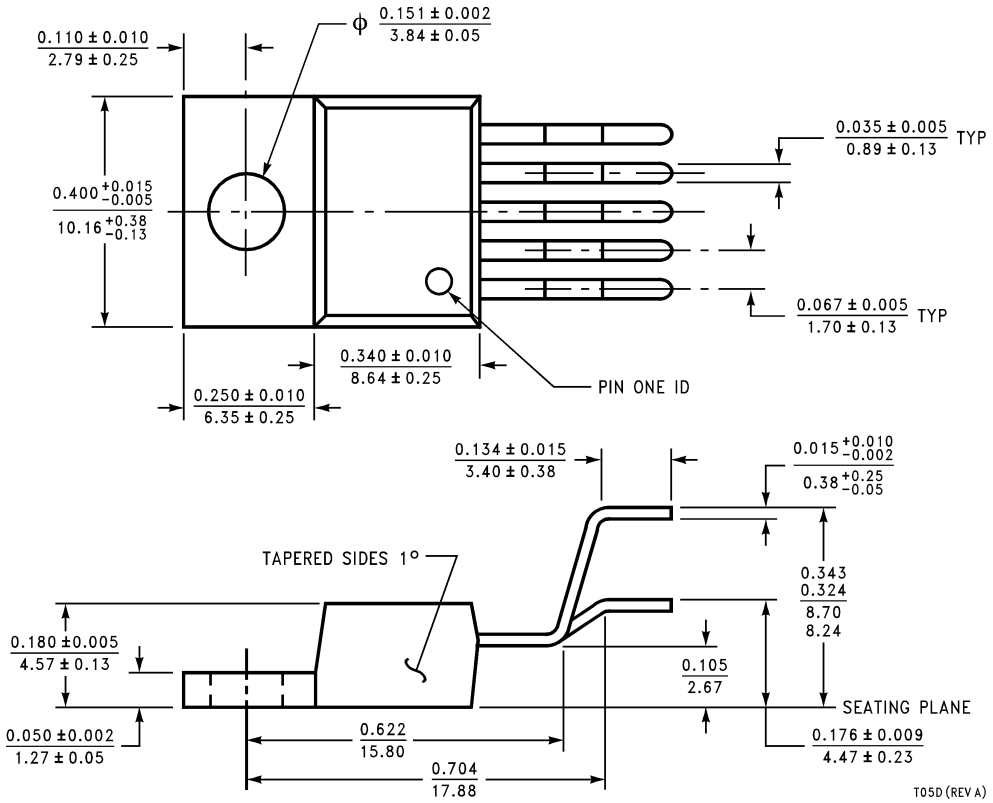
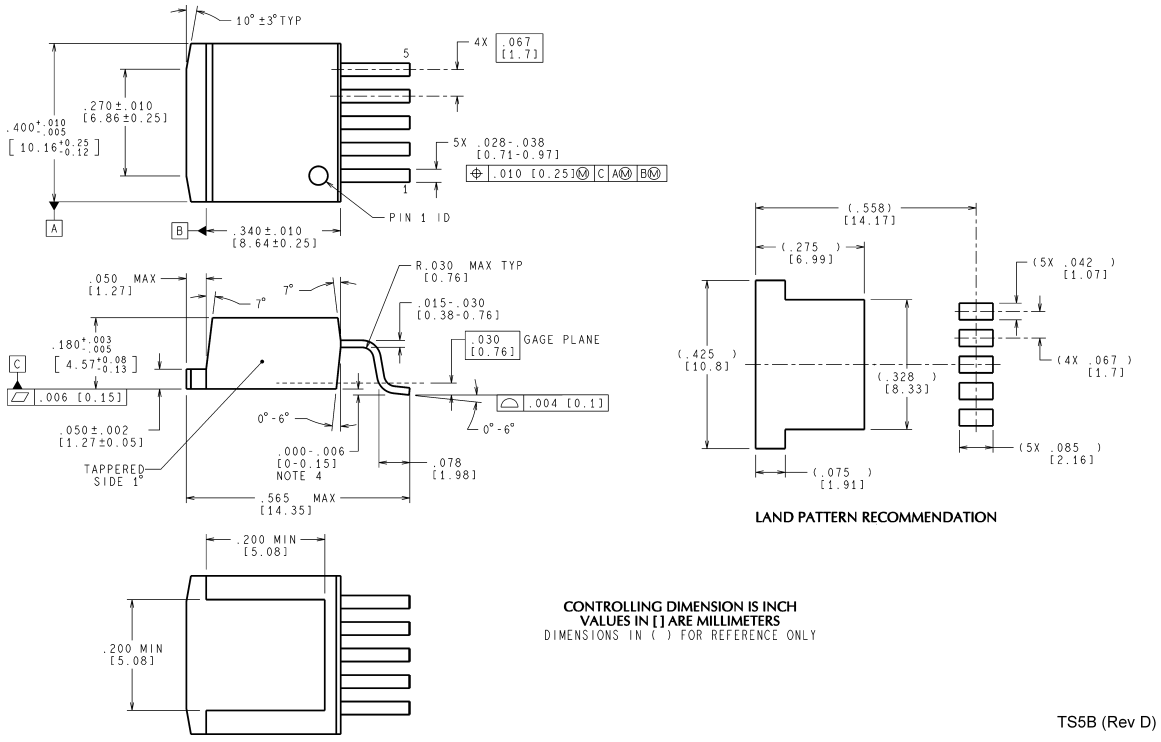


FIGURE 3. θ_{JA} vs. Copper (1 ounce) Area for PSOP Package

Physical Dimensions inches (millimeters) unless otherwise noted

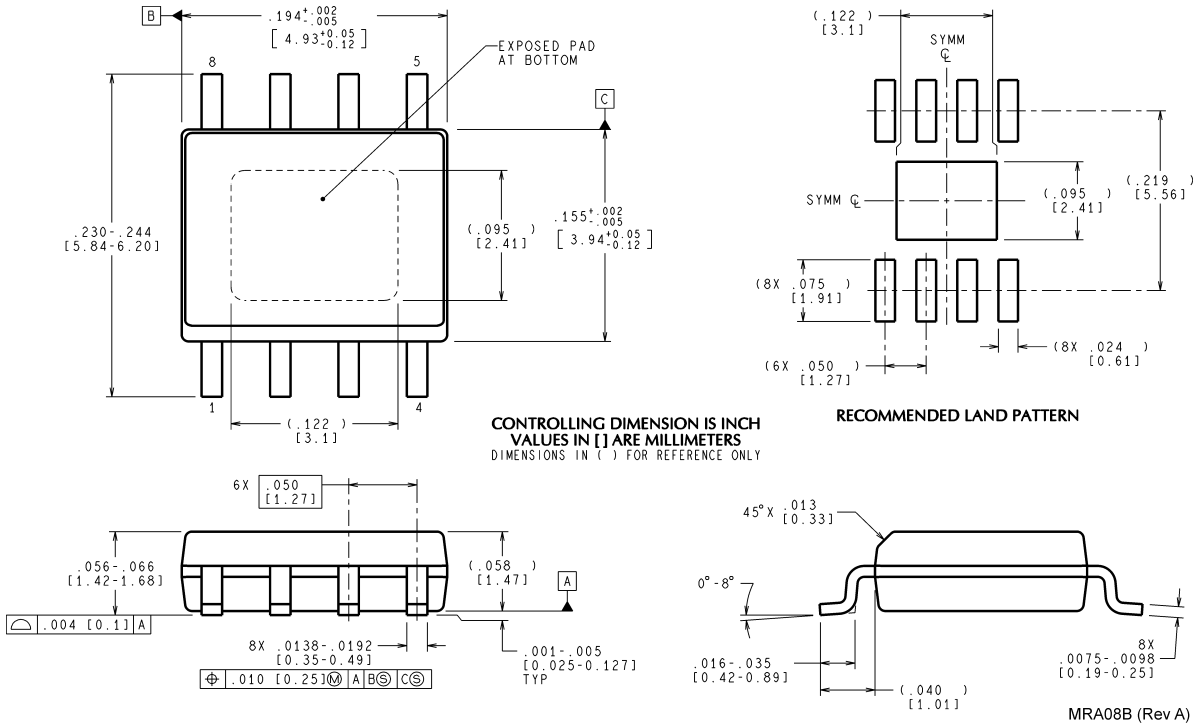


TO220 5-lead, Molded, Stagger Bend Package (TO220-5)
NS Package Number T05D



TO263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



PSOP 8-Lead, Molded, PSOP-2
NS Package Number MRA08B

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor follows the provisions of the Product Stewardship Guide for Customers (CSP-9-111C2) and Banned Substances and Materials of Interest Specification (CSP-9-111S2) for regulatory environmental compliance. Details may be found at: www.national.com/quality/green.

Lead free products are RoHS compliant.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560